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EXAMINER	
SILVER, DAVID	
ART UNIT	PAPER NUMBER
2128	

NOTIFICATION DATE	DELIVERY MODE
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

mailroom@bskb.com

Office Action Summary	Application No.	Applicant(s)	
	10/505,260	DALTON, DAMIAN	
	Examiner	Art Unit	
	DAVID SILVER	2128	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 May 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *66-78 and 80-129* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *66-78 and 80-129* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. The Instant Office Action is in response to a Request for Continued Examination filed 5/22/2008.

2. Claims 66-78 and 80-129 are currently pending in Instant Application.

Priority

3. Claim to priority have been acknowledged in previous Office Action **(2/22/02)**.

Response to Arguments

Response: 35 U.S.C. § 101

4. **Examiner Response:**

4.1 Applicants' amendments are sufficient to overcome the 35 U.S.C. § 101 rejections. Accordingly, the rejections have been withdrawn.

Response: 35 U.S.C. § 102

5. **Applicants argue:**

5.1 Dalton discloses a method in which an entire circuit is brought into the associative memory mechanism at the same time. However, Dalton does not disclose or suggest

> ***dividing the circuit representation into a plurality of circuit segments***, at least one of the circuit segments containing a plurality of logic gates;
>
> ***assigning a unique segment identifier to each segment;***
>
> generating a circuit segment table in the associative memory and storing the unique segment identifiers along with segment data in a circuit segment table;
>
> for a time period, identifying segments that have a state S0 in that time period based on the segment data stored in the circuit segment table;
>
> ***bringing only the segments with a state S0, one at a time***, into the associative memory mechanism from external memory for evaluation; and
>
> evaluating segments with a state S0, in the associative memory mechanism and storing a result of the evaluation in a tangible medium.

(Remarks: page 20)

6. **Examiner Response:**

6.1 Applicants' arguments are confusing as there is a lack of elaboration / specifics as to what is being argued. It appears Applicants' argument that, previously Dalton brought into the AMM the entire

circuit "at the same time", however, now, it is done "one at a time". Such argument is unpersuasive, for, at least the reasons set-forth in the Previous Office Action dated 4/23/2007, sections 28.1 and 28.2. Furthermore, attention is drawn **(page 60 lines 24 - last line)**.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

7. Claims 66-78, and 80-129 are rejected under 35 U.S.C. 102(b) as being anticipated by ***Damian Dalton*** WO 01/01298 A2 ("Dalton").

Dalton discloses: 66. A parallel processing method of logic event simulation on circuits comprising a plurality of logic gates, the logic gates having interconnect lines therebetween, the method being carried out in a main processor and an associative memory mechanism, the associative memory mechanism comprising a plurality of associative arrays and at least one result register, including an external memory and means to transfer data between the associative memory and the external memory, external to the associative memory mechanism, the method comprising the steps of **(page 13 lines 25-28 - files)**:

storing a circuit representation in external memory **(page 28 "axyla.dat is the data file defining the gate and model types in the circuit")**;

dividing the circuit representation into a plurality of circuit segments, at least one of the circuit segments containing a plurality of logic gates **(page: 2 lines 15-18 and page 60 lines 28-30)**;

assigning a unique segment identifier to each segment **(page 8 line 8: "forming a unique word in the associative memory mechanism")**;

generating a circuit segment table in the associative memory and storing the unique segment identifiers along with segment data in a circuit segment table **(pages: 16 line: 10-14; page 42 line 5: "Fan-out hdr table"; page 8 line 8)**;

for time period, identifying segments that have state S0 in that time period based on the segment data stored in the circuit segment table **(3 14-17; Fig 6 and texts which further expand**

on its features, page: 10 line: 27-28; page 55 lines 23-32);

bringing only the segments with a state S9, one at a time, into the associative memory mechanism from external memory for evaluation and evaluating the segments with a state S0, in the associative memory mechanism and storing a result of the evaluation, in a tangible medium **(page 60 lines 24-34; this is an inherent feature of the disclosed reference)**.

Dalton discloses: 67. A parallel processing method of logic event simulation as claimed in claim 66 in which the segment data stored in the circuit segment table comprises the maximum delay state of a segment, which indicates the maximum time delay in which any gate in the segment may make a transition **(page: 2 line: 4-6)**.

Dalton discloses: 68. A parallel processing method of logic event simulation as claimed in claim 66 in which the associative memory mechanism comprises a pair of associative arrays, associative array 1a and associative array 1b, an input value register bank and a hit list **(abstract, page: 1 line: 10-17)**.

Dalton discloses: 69. A parallel processing method of logic event simulation as claimed in claim 68 in which the circuit segment table data of associative array 1a, and associative array 1b and input value register bank are stored in external memory during segment evaluation **(page: 16 line: 15-26)**.

Dalton discloses: 70. A parallel processing method of logic event simulation as claimed in claim 66 in which after evaluation of a first segment the segment data of all the first segments fan-out gates are updated **(page: 16 line: 10-14, page: 20 line: 14-16: "fan-out gates are to be updated")**.

Dalton discloses: 71. A parallel processing method of logic event simulation as claimed in claim 70 in which when a new maximum delay state is greater than the previous maximum delay state of a fan-out segment, the segment data is updated with the new maximum delay state **(page: 20 line: 31-33: "The length of the delay word is ascertained and if the delay word width exceeds the associative.")**.

Dalton discloses: 72. A parallel processing method of logic event simulation as claimed in claim 66 in which inactive segments are not brought into the associative memory mechanism for evaluation until they have undergone an input change to a gate in that segment **(page: 4 line: 23-30, page 34 "If**

the current inspected bit is set, Hit_fndflag is asserted and the vector and the size (no. of gates) for the fan-out list loaded into Fan_out_src_reg and Fan_out_size_reg, respectively.").

Dalton discloses: 73. A parallel processing method of logic event simulation as claimed in claim 66 in which all interconnect lines are held in a segment dedicated to interconnect lines **(page: 11 line: 28-29)**.

Dalton discloses: 74. A parallel processing method of logic event simulation as claimed in claim 66 in which all logic gates of a particular type are held in segments with logic gates of the same type **(page: 11 line: 1-5)**.

Dalton discloses: 75. A parallel processing method of logic event simulation as claimed in claim 68 in which the segment table is an N.sub.s.times.M bits segment table where N.sub.s is equal to the number of segments and M is equal to the sum of the number of bits wide of associative array 1a, associative array 1b, input value register and the hit list **(page: 10 line: 2, page: 6 line: 25-30, code allocating space on page 31)**.

Dalton discloses: 76. A parallel processing method of logic event simulation as claimed in claim 68 in which at least portion of associative array 1a, associative array 1b, input value register bank and the hit list are used to store the segment table at all times **(page: 10 line: 2: "input value register bank", page: 12 line: 8-9)**.

Dalton discloses: 77. A parallel processing method of logic event simulation as claimed in claim 68 in which when gate evaluations are completed for a particular time interval the previous segment table history is stored in the associative array 1b **(page: 11 line: 18-20, page: 10 line: 28-29, page: 55 line: 23-25, page: 4 line: 30-35, page: 5 line: 21-25)**.

Dalton discloses: 78. A parallel processing method of logic event simulation as claimed in claim 68 in which the input value register bank is shifted into associative array 1b **(page: 10 line: 10)**, and associative array 1a contains the maximum state of each segment, test patterns are then applied to contents of array 1b to determine transitions to lower states **(bottom of page 38: "These parameters**

define the upper and lower limits of the segments of the Group-test Hit list").

Dalton discloses: 80. A parallel processing method of logic event simulation as claimed in claim 66 in which the minimum state of all segments, S.sub.STATEMIN, is calculated and all states are time advanced by S.sub.STATEMIN Time Units before evaluation of the segments commences **(bottom of page 38: "These parameters define the upper and lower limits of the segments of the Group-test Hit list")**.

Dalton discloses: 81. A parallel processing method of logic event simulation as claimed in claim 68 in which the set up time, T.sub.SETUP, of synchronous devices may be modelled where T.sub.setup=N.p+M, where N=integer, M=integer<P and P=bit width of array 1b, where by the following steps are performed:

the state entry of array 1a of a signal is set to S.sub.sn; a start marker is placed in the left most position of array 1b **(page: 21 line: 20-21)**;

array 1b is incremented in time and when start marker reaches the right-most position of array 1b and the signal has remained constant the state S.sub.sn is decremented to S.sub.sn-1, and the next time array 1b is incremented the start marker is returned to the left-most position in array 1b once again and array 1b is then incremented in the normal manner; the previous step is repeated until state entry S.sub.sn=S.sub.so, then the array 1b is incremented another M times **(page: 21 line: 20-21, page: 17 line: 28-29, page: 17 line: 19-25, page: 18 line: 10 - end of page)**; and

if the signal has remained constant for N.p+M time units then the state entry in array 1a is set to state setup, S.sub.SETUP **(page: 16 line: 5-7, page: 21 line: 30- page 22 line 10)**.

Dalton discloses: 82. A parallel processing method of logic event simulation as claimed in claim 68 in which the hold time, T.sub.HOLD, of synchronous devices may modelled where T.sub.hold=R.p+Q, and where R=integer, Q=integer<P and P=bit width of array 1b using the following steps:

when a clock makes a transition there is a search of state entries in array 1a to see if an input signal is in state S.sub.setup; any input signal in states in S.sub.setup are updated to the state S.sub.HR, and a start marker is placed in the left-most position of array 1b, array 1b is incremented and until the

marker has made its way to the right-most position in array 1b and the signal has remained constant **(page: 21 line: 20-21)**;

the state is decremented to S.sub.HR-1, the start marker is returned to the left-most position in array 1b the next time that array 1b is incremented, array 1b is then incremented in the normal manner and this is continued until the state is equal to S.sub.Ho,; when S.sub.HR=S.sub.HO then the array 1b is incremented a further Q times **(page: 21 line: 20-21, page: 17 line: 28-29, page: 17 line: 19-25, page: 18 line: 10 - end of page)**;

on the signal remaining constant over the entire period then the signal state is updated to S.sub.HOLD and the output value of the synchronous device is ascertained **(page: 16 line: 5-7, page: 21 line: 30- page 22 line 10)**.

Dalton discloses: 83. A parallel processing method of logic event simulation as claimed in claim 82 in which if the output value of the device has changed it is propagated to the fan-out list of the device **(page: 1 line: 5-20: "propagated to fan out gates")**.

Dalton discloses: 84. A parallel processing method of logic event simulation as claimed in claim 81 in which successive states are generated by causing a shift right operation in array 1a **(page: 17 line: 30-34: "process of updating the signal values of a particular wire is achieved by shifting right by one time unit all values")**.

Dalton discloses: 85. A parallel processing method of logic event simulation as claimed in claim 66 in which there is provided an amended result registering mechanism in which when a number of tests are carried out on a gate pair the result of each test is sent to a result register where on completion of all the tests the result register will indicate that all tests were successful or that at least one was unsuccessful **(page: 13 line: 19, page: 11 line: 10)**.

Dalton discloses: 86. A parallel processing method of logic event simulation as claimed in claim 85 in which the result register comprises an adder **(this is an inherent feature of Dalton's teachings)**.

Dalton discloses: 87. A parallel processing method of logic event simulation as claimed in claim 85 in which the result register is a bi-state device **(this is an inherent feature of Dalton's teachings)**.

Dalton discloses: 89. A parallel processing method of logic event simulation as claimed in claim 87 in which the result register on start-up is supplied with an appropriate priming input instead of last result so that it is ready to receive the first result **(this is an inherent feature of Dalton's teachings)**.

Dalton discloses: 90. A parallel processing method of logic event simulation as claimed claim 85 in which the amended result registering mechanism further comprises a result polarity circuit to invert a result and ensure a logic 1 is applied to the result register if the correct response to a test was for the test to be failed **(page: 13 line: 19)**.

Dalton discloses: 91. A parallel processing method of logic event simulation as claimed in claim 90 in which the result polarity circuit comprises a pair of AND gates, a pair of inverters and an OR gate, a result polarity control is fed to each of the AND gates, the other input of each of the AND gates being provided by the result of a test carried out on a gate pair, the inverters inverting the two inputs to one of the AND gates, the outputs of the AND gates being fed directly to the OR gate **(inherent in associative memory parallel searching, which is disclosed by the reference)**.

Dalton discloses: 92. A parallel processing method of logic event simulation as claimed in claim 85 in which the amended result registering mechanism is further provided with a logic combination circuit to determine whether an output gate pair of array 1b are ANDed or ORed together **(page: 18 line: 26-35)**.

Dalton discloses: 93. A parallel processing method of logic event simulation as claimed in claim 92 in which the logic combination circuit further comprises three AND gates and a logic combination circuit control, the logic combination circuit control being anded individually with each output of an array 1b gate pair and the gate pair anded in the third AND gate, when the logic combination requires an AND operation to be carried out, logic combination circuit control is given a value 0 and if an OR operation is required logic combination circuit control is given a logic value 1 **(inherent in associative memory parallel searching, disclosed by the reference)**.

Dalton discloses: 94. A parallel processing method of logic event simulation as claimed in claim 93 in which the logic combination circuit further comprises an OR gate, each of the outputs of the three AND

gates being fed to the OR gate **(page: 18 line: 26-35; inherent)**.

Dalton discloses: 95. A parallel processing method of logic event simulation as claimed in claim 94 in which the output of the OR gate is led to the result polarity circuit as the result of a test carried out on a gate pair **(page: 18 line: 26-35; inherent)**.

Dalton discloses: 96. A parallel processing method of logic event simulation as claimed in claim 85 in which there is provided an amended result registering mechanism for each gate pair **(page: 11 line: 24-25)**.

Dalton discloses: 97. A parallel processing method of logic event simulation as claimed in claim 66 in which when all active segments have a state>S0, a check of all segment states is made until the lowest segment state S.sub.min is found, then each segment state is decremented by S.sub.min in order to advance simulation to the next evaluation stage **(page: 12 line: 4-6)**.

Dalton discloses: 98. A parallel processing method of logic event simulation as claimed in claim 97 in which the lowest state value is stored in a low global register each time there is a gate state change, if a new state is less than the lowest state value, the lowest state value in the low global register is replaced by the new state. **(page: 16 line: 1-8)**.

Dalton discloses: 99. A parallel processing method of logic event simulation as claimed in claim 66 in which there is provided a scan system comprising a priority decoder and a shift register **(page: 57 line: 10-15)**.

Dalton discloses: 100. A parallel processing method of logic event simulation as claimed in claim 66 in which there is provided a segment address table and the segment address table is divided into a number of rows, each row being M bits long, and each segment address is stored in the M-D bits of the segment row when the number of segments=2.sup.D **(inherent)**.

As per claims 101-126, note the rejection of claims 66-70, 73-75, 81-83, 85-90, 92-95, 97-99, 85, and 100 above, respectively. The Instant Claims are functionally equivalent to the above-rejected claims and are therefore rejected under same prior-art teachings.

Dalton discloses: 127. A processor as claimed in claim 101 in which the processor is embodied in

computer readable format are stored in a physical carrier **(code on pages 28-54)**.

Dalton discloses: 128. A processor as claimed in claim 127 in which the processor in computer readable format may be stored on a disc **(page: 13 line: 27: file; code on pages 28-54)**.

Dalton discloses: 129. A processor as claimed in claim 127 in which the processor in computer readable format may be stored on a record medium **(page: 13 line: 27: file; code on pages 28-54)**.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

8. Claims 66-68 and 101-103 are rejected under 35 U.S.C. 103(a) as being unpatentable over Damian Dalton "An Associative Memory Approach to Parallel Logic Event-driven Simulation" ("Dalton"), and further in view of Official Notice taken (taken as Admitted Prior art for lack of adequate traversal per MPEP 2144.03 ("If applicant does not traverse the examiner's assertion of official notice or applicant's traverse is not adequate, the examiner should clearly indicate in the next Office action that the common knowledge or well-known in the art statement is taken to be admitted prior art because applicant either failed to traverse the examiner's assertion of official notice or that the traverse was inadequate. If the traverse was inadequate, the examiner should include an explanation as to why it was inadequate.")).

Dalton discloses claim 66: A parallel processing method of logic event simulation on circuits comprising a plurality of logic gates, the logic gates having interconnect lines therebetween, the method being carried out in a main processor and an associative memory mechanism, the associative memory mechanism comprising a plurality of associative arrays and at least one result register **(abstract; page 344**

annotation "register"), characterized in that: dividing the circuit representation into a plurality of circuit segments, at least one of the circuit segments containing a plurality of logic gates **(page 341 col 2 annotated "partition")**; assigning a unique segment identifier to each segment **(page 344 and 345 annotation "unique id")**; generating a circuit segment table in the associative memory and storing the unique segment identifiers along with segment data in a circuit segment table **(page 344 annotation "associated memory" and page 345 annotated "assoc. memory")**; for each time period, identifying segments that are have a state S0 in that time period based on the segment data stored in the circuit segment table **(page 345 annotated "ident. of active" and page 342 annotated "id. of active")**; bringing only the segments with a state S0, one at a time, into the associative memory mechanism from external memory for evaluation **(this is an inherent step in the disclosed reference)**; and evaluating the active segments in the associative memory mechanism and storing a result of the evaluation **(page 344 col 1 first paragraph; last sentence (item (ii)))**.

Dalton however does not expressly disclose there is provided an external memory and means to transfer data between the associative memory and the external memory, external to the associative memory mechanism, the method comprising the above mentioned steps and storing a circuit representation in external memory. Official Notice is taken with respect to this limitation. Specifically, Dalton discusses the use of circuit models and the simulation thereof. Circuit models can range from very simple to very complex. When the circuit models are complex it is unrealistic and at times impossible to manually input the models each time a simulation is performed. Therefore, external memory (external storage) is used. Such external memory can be, for example, a harddrive and a file thereon which contain the model. It would have been obvious to one of ordinary skill in the art to combine the features in order to create a faster simulation by not having to manually re-generate the circuit model each time a simulation is performed, and by using an already-made circuit model. Thus, saving the time and money associated with regenerating the circuit model by saving it to an external memory element (such as a harddisk drive).

Dalton discloses: 67. A parallel processing method of logic event simulation as claimed in claim 66 in

which the segment data stored in the circuit segment table comprises the maximum delay state of a segment, which indicates the maximum time delay in which any gate in the segment may make a transition **(page 342 annotations "item predefined units of time" and "delay models"; page 343 annotation "delay models")**.

Dalton discloses: 68. A parallel processing method of logic event simulation as claimed in claim 66 in which the associative memory mechanism comprises a pair of associative arrays, associative array 1a and associative array 1b, an input value register bank and a hit list **(page 344 annotation "associative memory"; page 345 "assoc. memory" and "hit list")**.

As per claim(s) 101-103, note the rejection of claim(s) 66-68 above. The Instant Claim(s) is/are functionally equivalent to the above-rejected claim(s) and is/are therefore rejected under same prior-art teachings.

Support for Amendments and Newly Added Claims

9. Applicants are respectfully requested, in the event of an amendment to claims or submission of new claims, that such claims and their limitations be directly mapped to the specification, which provides support for the subject matter. This will assist in expediting compact prosecution. MPEP 714.02 recites: "Applicant should also specifically point out the support for any amendments made to the disclosure. See MPEP § 2163.06. An amendment which does not comply with the provisions of 37 CFR 1.121(b), (c), (d), and (h) may be held not fully responsive. See MPEP § 714." **Amendments not pointing to specific support in the disclosure may be deemed as not complying with provisions of 37 C.F.R. 1.131(b), (c), (d), and (h) and therefore held not fully responsive.** Generic statements such as "Applicants believe no new matter has been introduced" may be deemed insufficient.

Requests for Interview

10. In accordance with 37 CFR 1.133(a)(3), requests for interview must be made in advance. Interview requests are to be made by telephone (571-272-8634) call or FAX (571-273-8634). Applicants must provide a detailed agenda as to what will be discussed (generic statement such as

"discuss §102 rejection" or "discuss rejections of claims 1-3" may be denied interview).

The detail agenda along with any proposed amendments is to be written on a PTOL-413A or a custom form and should be faxed (or emailed, subject to MPEP 713.01.I / MPEP 502.03) to the Examiner at least 3 days prior to the scheduled interview.

11. Interview requests submitted within amendments may be denied because the Examiner was not notified, in advance, of the Applicant Initiated Interview Request and due to time constraints may not be able to review the interview request to prior to the mailing of the next Office Action.

Conclusion

12. All claims are rejected.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to David Silver whose telephone number is (571) 272-8634. The examiner can normally be reached on Monday thru Friday, 10am to 6:30pm. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kamini Shah can be reached on 571-272-2279. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

/Kamini S Shah/

Supervisory Patent Examiner, Art Unit 2128

/ DS /

David Silver, Patent Examiner
Art Unit 2128